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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 :		(11) International Publication Number:
H01L 21/70, 21/20	A1	WO 93/01617
		(43) International Publication Date: 21 January 1993 (21.01.93)

(21) International Application Number: PCT/SE92/00390

(22) International Filing Date: 9 June 1992 (09.06.92)

(30) Priority data:
725,814 8 July 1991 (08.07.91) US

(71) Applicant *(for all designated States except US)*: ASEA BROWN BOVERI AB [SE/SE]; S-721 83 Västerås (SE).

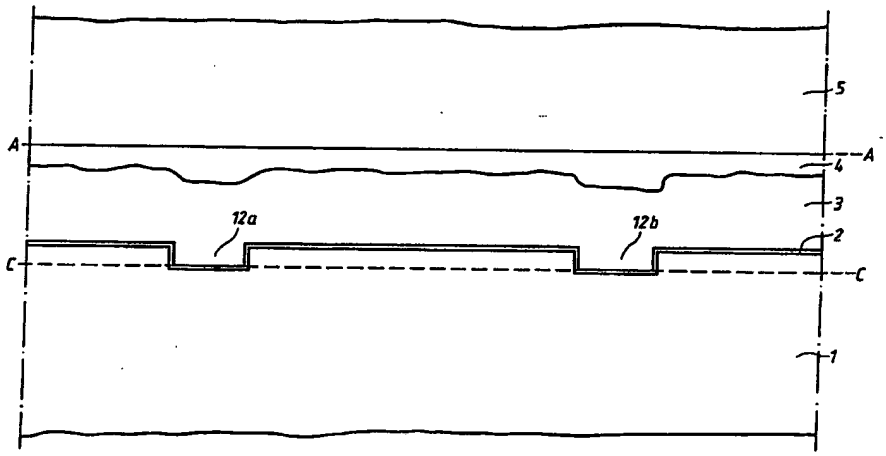
(72) Inventor; and
(75) Inventor/Applicant *(for US only)* : SVEDBERG, Per [SE/SE]; Björnskogsgränd 13, S-162 46 Vällingby (SE).

(74) Agent: WARSTRAND, Hans; ABB Corporate Research, Patent Department, S-721 78 Västerås (SE).

(81) Designated States: JP, US, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LU, MC, NL, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: METHOD FOR THE MANUFACTURE OF A SEMICONDUCTOR COMPONENT



(57) Abstract

A semiconductor component may be manufactured by forming in a surface of a silicon body (1) a number of recessed surface portions having essentially plane bottom surfaces and a predetermined depth, deposing on said surface, including said recesses, a diamond layer (3) having a thickness exceeding the depth of said recessed surface portions, said diamond layer having first surface parts (12a, 12b) adjoining the bottoms of said recesses, bonding said silicon body to said substrate with said diamond layer facing the substrate, removing parts of said silicon body distant from said substrate down to a plane (C-C) determined by the surfaces of said first parts (12a, 12b) of said diamond layer.

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Method for the Manufacture of a Semiconductor Component

Technical Field

The present invention relates to a method for the manufacture of a semiconductor component, said component having a substrate, a diamond layer on said substrate, and at least one active silicon layer on said diamond layer, at least one semiconductor circuit component being formed in said active silicon layer.

Background Art

It is known to manufacture single semiconductor components and integrated circuits in the so-called SOI technology, which results in a great flexibility in the design and use of the components or circuits by their being electrically insulated from the substrate and from each other. In said technology the component or circuit is formed in a layer of semiconducting material, usually silicon, which layer is arranged on an electrically insulating substrate. This substrate usually is a body of semiconductor material, for instance silicon, having an electrically insulating layer, such as silicon dioxide, upon which the active silicon layer is arranged. In order to obtain a sufficient electrical insulation between the substrate and the component or circuit, the silicon dioxide layer has to be relatively thick, typically at least one or a few µm. Silicon dioxide does, however, have poor thermal properties, especially a low thermal conductivity. This fact results in components of this kind having a limited power handling capacity. Further, such components are sensitive to radioactive (ionizing) radiation. Such radiation results in the formation of electron-hole pairs in the oxide layer, the holes remaining in the oxide and causing a charging-up of the oxide layer, and also resulting in surface states at the junction between the active silicon layer and the oxide layer. Both these phenomena influence in a negative manner the function of the

component or circuit formed in the active silicon layer.

It is also known that diamond is a material combining good electrical insulation with a high thermal conductivity and a high thermal capacity. It has therefore been proposed to use diamond as a substrate, or to use a diamond layer as electrical insulation between a substrate and active semiconductor layers. The direct junction beween the diamond material and the active silicon layer has, however, proved to cause insufficiently controlled surface states, which will influence in a negative manner the function of the components or circuits formed in the active layer.

Prior art components of this kind have required complicated manufacturing processes. It has been difficult to achieve a closely controlled thickness of the active silicon layer, and therefore it has been difficult or impossible to manufacture components with thin active layers. Some of the processes used have also tended to generate defects in the active layer. In those cases where the active layer (or several separate active layers) has or have been deposited on the diamond layer various so-called corner effects (such as increased electrical fields or crystal defects) have been hard to avoid at the edges of the layer or layers.

Disclosure of the Invention

The present invention has as an object to obtain a simple and advantageous method for manufacturing semiconductor components of the kind initially referred to.

A further object is to obtain a manufacturing method, by the use of which a closely controlled thickness of the active layer or layers may be achieved in a simple manner, and which method makes it possible to manufacture very thin active layers.

Another object is to obtain a manufacturing method which results in a component, in which the so-called corner

effects are avoided at the edges of the active layers. A further object of the invention is to obtain a manufacturing method which gives a component with a high resistance against radiation effects (good radiation hardness).

Brief Description of the Drawings

A preferred embodiment of the invention will be described below referring to the enclosed drawings 1-3, which illustrate various stages of the manufacturing process. Figure 1 shows the silicon body, which is to form the active layers, after the generation of a diamond layer and a polycrystalline silicon layer. Figure 2 shows the assembly generated by bonding the silicon body to the substrate. Figure 3 shows the final assembly before separation into individual components.

Description of the Preferred Embodiments

According to a preferred embodiment of the invention the manufacture is started with a body 1 of monocrystalline silicon, which has a plane surface (the upper surface in figure 1). Recesses 1a, 1b etc are formed in a surface of the body. The recesses form a square lattice. The silicon remaining between the recesses forms square mesas 10a, 10b, 10c etc. Each mesa will eventually form an active silicon layer. The lateral dimensions of the mesas are adapted to the component, the components, or to the integrated circuit to be formed in the mesa. The same applies to the height of the mesas, which is equal to the depth of the recesses 1a, 1b etc. A typical mesa may have the form of a square with the length of its sides being between10 µm and 1 mm. The depth of the recesses, that is, the height of the mesas eventually to be formed, may typically be 0.5 µm. The width of the recesses may be 2 - 10 µm.

The recesses are formed by etching, using, for instance, conventional photolitographic technology to define the parts to be etched and masking those parts of the surface not to

be etched.

After the etching procedure a thin layer 2 of silicon dioxide is formed on the surface of the silicon body. This layer prevents direct contact between the active silicon layer and the diamond layer in the finished component, thereby preventing or reducing undesirable surface states. The oxide layer 2 is preferably thin in order to reduce the formation of charge carriers in the layer if the component is subjected to radiation. The thickness of the layer is preferably not greater than 0.02 µm, and it should not exceed 0.05 µm.

The oxide layer 2 may be generated by thermal oxidation of the silicon in a moist oxygen atmosphere, followed by a heat treatment in an inert atmosphere. This method has proved to result in a low tendency of formation or capture of charge carriers in the oxide layer when the component is subjected to radiation.

As the next step a polycrystalline diamond layer 3 is formed on the oxide layer 2. The diamond layer may advantageously be formed by a so-called hot wire CVD technique. Alternatively a so-called plasma jet technique may be used for the formation of the diamond layer. The thickness of the diamond layer should exceed the depth of the recesses 1a, 1b etc. A typical thickness could be between 1.0 µm and 20 µm.

Thereafter a layer 4 of polycrystalline silicon is grown on the surface of the diamond layer 3 by means of any of several well-known methods. As the formation of such a layer is typically a slow and therefore expensive process, the thickness of the polycrystalline silicon layer 4 is preferably kept as low as possible. The primary function of this layer is to accommodate unavoidable surface unevenness of the diamond layer, and to make it possible to obtain the very plane and smooth surface neccessary for the subsequent bonding to the substrate. The thickness of the polysilicon layer 4 should not be greater than necessary to achieve this

object. A typical thickness could be 6µm. The required thickness of layer 4 may be reduced by grinding and/or polishing the surface of the diamond layer 3 to a high degree of planeness and evenness before application of the polysilicon layer 4.

After these process stages the state of the silicon body 1 with the layers applied thereon is the one shown in figure 1.

As the next step the surface of the polysilicon layer 4 is ground and/or polished in order to give the surface the high degree of planeness and surface finish necessary for the subsequent bonding to the substrate. After this operation the surface will be the one shown by the dashed line A-A in figure 1.

Figure 2 shows the silicon body 1 with the finished surface A-A. A substrate in the form of a silicon body 5 is applied to the body 1 or, rather, to the surface of the layer 4 applied to that body. That surface of the substrate 5 which faces layer 4 is, just as the surface of layer 4, brought to a high degree of planeness and surface smoothness by means of grinding and/or polishing. After applying said surfaces against each other the assembly is subjected to a heat treatment in a known manner, causing so-called thermal bonding between the surfaces.

As the next step the body 1 is removed, by grinding and/or polishing or other suitable method, to a depth determined by the plane C-C defined by the surfaces of those parts of the diamond layer 3, which are situated in the recesses 1a, 1b etc. These parts of the diamond layer will, due to the great hardness of the diamond material, function as an automatic stop for the grinding/polishing procedure. The material removal will automatically stop when the above-mentioned parts of the diamond layer are reached. In this manner the thickness of the active layers is automatically controlled to a high accuracy, and this desired thickness will be

accurately obtained by means of a simple grinding/polishing operation. Also, the material removal may be made in such a manner as to introduce only minimum defects in the remaining active silicon layers

Figure 3 shows the assembly after the removal of the body 1 down to the plane C-C (this figure shows the assembly turned upside down in relation to its position in figures 1 and 2). The active layers 12a, 12b have the form of squares, separated by a continuous lattice of diamond ridges. As each active layer is laterally completely surrounded by the diamond material, the above-mentioned corner effects are completely eliminated.

After this, the desired semiconductor circuits and/or components are formed in the active layers by conventional steps. Each active layer may comprise anything from one single component, such as a single transistor, up to one or more complicated integrated circuits.

As a final step the assembly shown in figure 3 is divided into separate components, typically with one active layer per component. Division lines B1-B1 and B2-B2 are shown in figure 3. The division is preferably done in a conventional manner by scribing the component surface and breaking it along the scribed lines. It may be advantageous to remove those parts of the diamond ridges, which are situated along the intended scribing lines, before the scribing and breaking operation.

It should be pointed out that the figures are intended to illustrate the principle of the invention, and the dimensions etc shown in the figures are not necessarily shown to scale.

A component according to the invention may comprise additional layers than those shown in the figures. For instance, a thin layer of a suitable material may be applied to the diamond layer 3 before application of the polysilicon layer

4 in order to improve the adhesion between these layers.

The polycrystalline silicon layer 4 may alternatively be a layer of amorphous silicon.

In the preferred embodiment described above the etched grooves 1a, 1b etc (figure 1) form a continuous square lattice, and the active layers of the final product will therefore have the form of squares. Alternatively, by selecting another shape of the lattice formed by the grooves, the active layers may be geiven rectangular form

In an alternative method according to the invention a layer of a suitable glass with a low melting point may replace the polysilicon layer 4. Such a glass may be a phosphorus-silicon oxide glass with 4% phosphorus having a softening point at approximately 1050 degrees centigrade.The phosphorus glass layer is planarized by heating the body 1 to the softening point of the glass. Thereafter the substrate 5 can be bonded to the body 1. The bond is further strengthened by another heat treatment close to the softening point. As the thermal conductivity of glass is lower than that of silicon, the glass layer should be as thin as possible in order not to impede the heat transfer from the active layers to the substrate.

In the preferred embodiment described above the etched grooves 1a, 1b etc (figure 1) form a continuous square lattice, and the final product as shown in figure 3 has a plurality of separate active layers 11a, 11b, 11c etc separated by the diamond ridges 12a, 12b etc, which form a continuous lattice. Alternatively the recesses etched in the surface of the silicon body 1 may be separate from each other, for instance constitute a plurality of square recesses. In the final product as shown in figure 3 the active silicon layer will then be a continuous layer with a plurality of separate diamond mesas reaching the surface.

Claims

1. A method for the manufacture of a semiconductor component, said component having a substrate (5), a diamond layer (3) on said substrate, and at least one active silicon layer (11a, 11b) on said diamond layer, at least one semiconductor circuit component being formed in said active silicon layer, said method comprising the steps of

forming in a surface of a silicon body (1) a number of recessed surface portions (1a, 1b) having essentially plane bottom surfaces and a predetermined depth,

depositing on said surface, including said recesses, a diamond layer (3) having a thickness exceeding the depth of said recessed surface portions, said diamond layer having first surface parts (12a, 12b) adjoining the bottoms of said recesses,

bonding said silicon body to said substrate with said diamond layer facing the substrate,

removing parts of said silicon body distant from said substrate down to a plane (C-C) determined by the surfaces of said first parts (12a, 12b) of said diamond layer.

2. A method according to claim 1, which includes the step of forming a layer of silicon dioxide (2) on said surface of said silicon body (1) after forming said recesses and before depositing said diamond layer.

3. A method according to claim 2, said silicon dioxide layer (2) having a thickness not exceeding 0.05 μm.

4. A method according to claim 1, including the step of depositing a layer (4) of polycrystalline silicon on the surface af said diamond layer (3) before the bonding of said silicon body (1) to said substrate (5).

5. A method according to claim 4, including the step of forming a plane surface (A-A) with a high surface finish on said polycrystalline silicon layer (4).

6. A method according to claim 5, including the step of polishing the surface of said polycrystalline silicon layer (4).

7. A method according to claim 4, said polycrystalline silicon layer (4) having a thickness not exceeding 10 µm.

8 A method according to claim 1, including the steps of

forming on the surface of said diamond layer (3) a layer of glass,

planarizing said glass layer by heating to the softening point of the glass, and thereafter

bonding said body to said substrate.

9. A method according to claim 1, said diamond layer (3) having a thickness of at least 1 µm.

10. A semiconductor component having a substrate (5), a diamond layer (3) bonded to said substrate, and an active silicon layer (11b) adjacent to a surface (C-C) opposed to said substrate and separated from the substrate by the diamond layer, wherein parts (12a, 12b) of said diamond layer (3) extend to said surface.

11. A semiconductor component according to claim 10, in which said active layer (11b) is completely surrounded by parts (12a, 12b) of said diamond layer (3) extending to said surface (C-C).

12. A semiconductor component according to claim 10,

comprising a layer of silicon dioxide (2) between said diamond layer (3) and said active layer (11b).

13. A semiconductor component according to claim 12, said silicon dioxide layer (2) having a thickness not exceeding 0.05 µm.

14. A semiconductor component according to claim 10, said diamond layer (3) having a thickness of at least 1 µm.

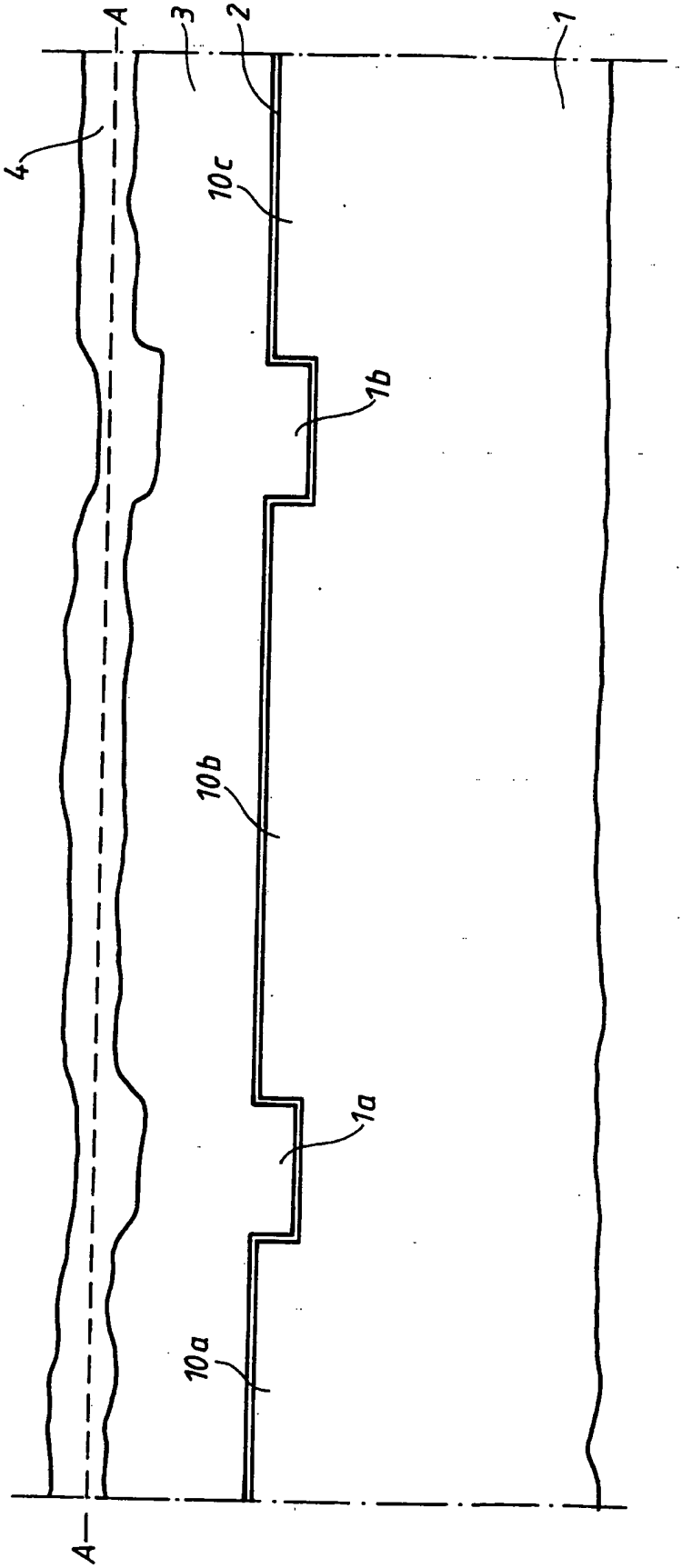

Fig. 1

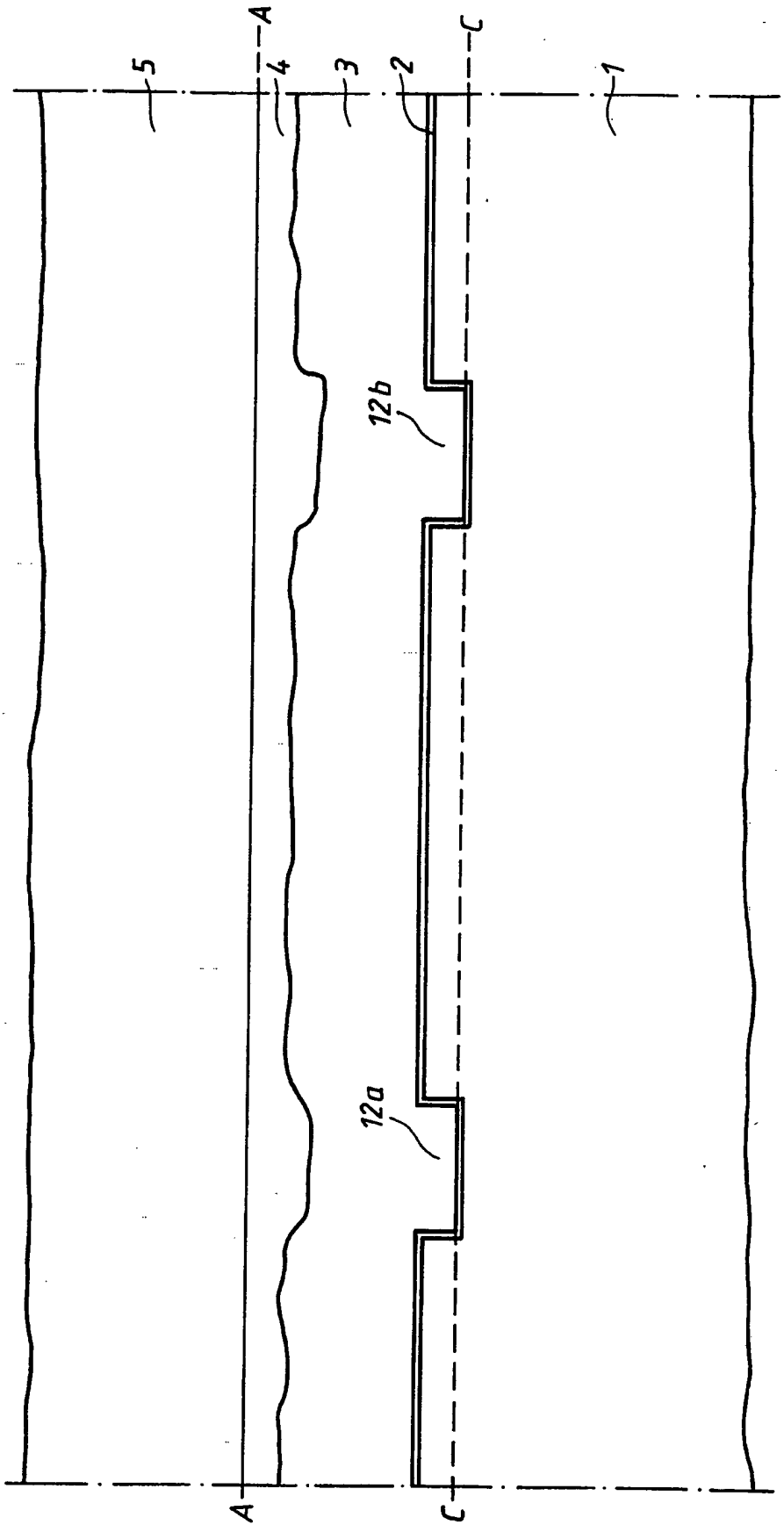

Fig. 2

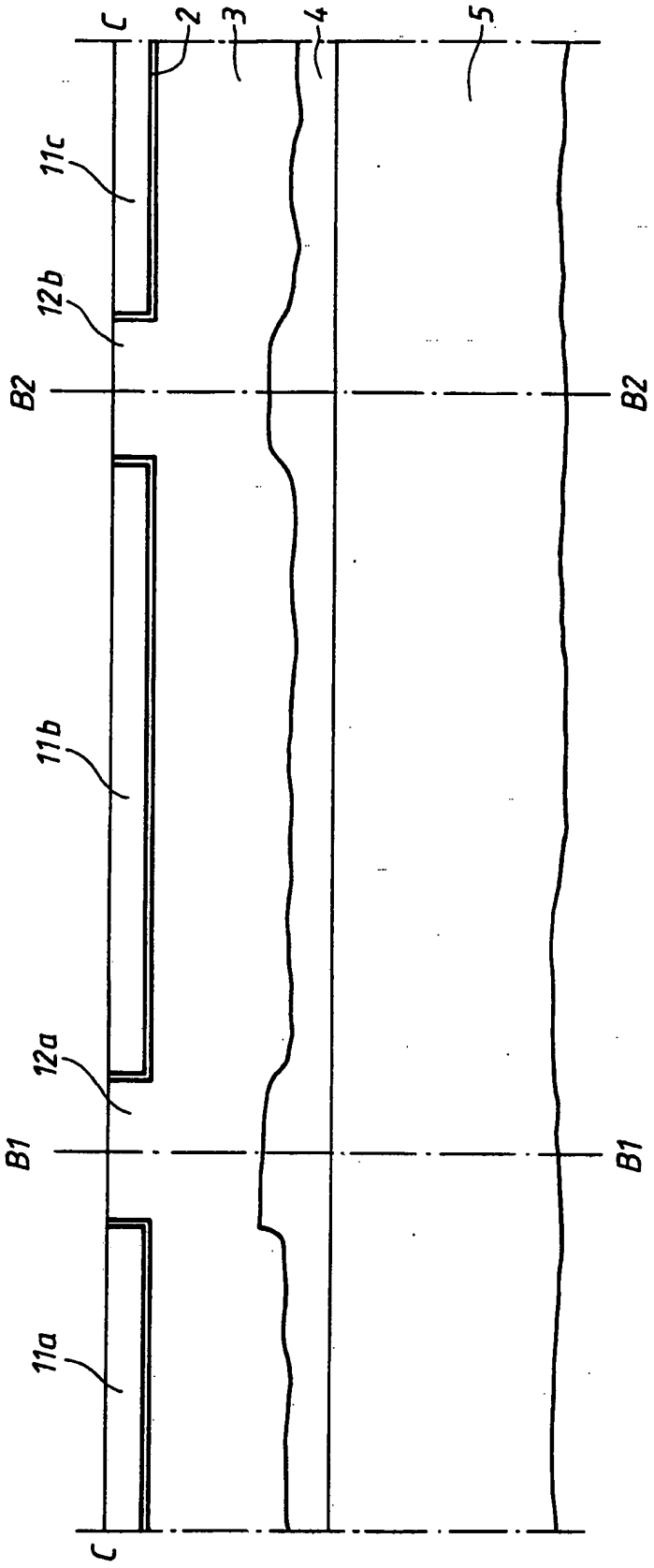

Fig. 3

INTERNATIONAL SEARCH REPORT

International Application No PCT/SE 92/00390

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC5: H 01 L 21/70, 21/20

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
IPC5	H 01 L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in Fields Searched[8]

SE,DK,FI,NO classes as above

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category *	Citation of Document,[11] with indication, where appropriate, of the relevant passages[12]	Relevant to Claim No.[13]
X	EP, A2, 0317124 (CRYSTALLUME) 24 May 1989, see column 4, line 48 - column 5, line 40; figures 2,3	10-11
Y		12-14
A		1-9
	--	
P,Y	WO, A1, 9111822 (ASEA BROWN BOVERI AB) 8 August 1991, see the whole document	10-14
P,A		1-9
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Y	APPL. PHYS. LETT., 56, No 23, June 1990 M.I. LANDSTRASS ET AL: "TOTAL DOSE RADIATION HARDNESS OF DIAMOND-BASED SILICON-ON-INSULATOR STRUCTURES", see page 2316 - page 2318	10-14
A		1-9
	--	

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
9th November 1992	10-11-1992
International Searching Authority	**Signature of Authorized Officer**
SWEDISH PATENT OFFICE	STIG EDHBORG

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ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. PCT/SE 92/00390

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the Swedish Patent Office EDP file on 30/09/92
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